WHAT IS CLAIMED IS:

1. A method for manufacturing an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising steps of :

providing a silicone substrate;

forming a select gate on said silicone substrate;

growing a tunnel oxide layer on exposed surfaces of said silicon substrate;

forming a floating gate self-aligned to one side of said select gate;

performing an ion implantation to form a source region and a drain region on said silicone substrate; and

forming a control gate over said floating gate and said select gate, wherein said control gate, said floating gate and said select gate are insulated from one another.

2. The method according to claim 1, wherein a select gate is formed by depositing a dielectric layer over a conductive layer.

3. The method according to claim 1, wherein said tunnel oxide layer is formed by performing a thermal oxidation process.

4. A method for manufacturing an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising steps of :

(a) providing a substrate and forming a first dielectric layer thereon;

(b) forming a first conductive layer and a second dielectric layer in sequence on said first dielectric layer;

(c) applying a first photolithography and etching process on said second dielectric layer and said first conductive layer to form a select gate;

(d) forming a third dielectric layer on said first dielectric layer, said second dielectric layer and said select gate;

(e) applying a first anisotropic etching process on said third dielectric layer to form a sidewall beside said select gate;

(f) removing said first dielectric layer to expose said silicone substrate;

(g) growing a tunnel oxide layer on said exposed surfaces of said silicon substrate, and then forming a second conductive layer on said tunnel oxide layer, said sidewall and said select gate;

(h) applying a second anisotropic etching process on said second conductive layer to form a spacer adjacent to said sidewall of said select gate,

(i) applying a second photolithography and etching process on said spacer to strip said spacer uncovered by a photo-resistance and, subsequently forming a floating gate self-aligned to one side of said select gate;

(j) forming a fourth dielectric layer on said tunnel oxide layer, said select gate, said sidewall and said floating gate;

(k) performing an ion implantation to form a source region and a drain region on said silicone substrate;

(l) forming a third conductive layer on said fourth conductive layer; and

(m) applying a third photolithography and etching process to form a control gate, wherein said control gate and said floating gate is separated by said fourth dielectric layer.

5. The method according to claim 4, wherein said substrate is a silicone substrate.

6. The method according to claim 4, wherein said tunnel oxide layer is formed by performing a thermal oxidation process.

7. The method according to Claim 4, wherein each of said first dielectric

layer, said second dielectric layer, said third dielectric layer and said fourth dielectric layer is one selected from a group consisting of silicon oxide, silicon nitride and silicon oxide/nitride composite.

8. The method according to claim 4, wherein said first conductive layer is one selected from a group consisting of polysilicon, amorphous silicon, recrystallized silicon and polycide.

9. The method according to claim 4, wherein each of said second conductive layer and said third conductive layer is one selected from a group consisting of polysilicon, amorphous silicon and recrystallized silicon.

10. The method according to claim 4, wherein each of said first anisotropic etching process and said second anisotropic etching process is a dry etching process.

11. A structure of an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising:

a silicone substrate having a source/drain region;

a tunnel oxide layer disposed over said silicone substrate;

a select gate disposed over said tunnel oxide layer, wherein said select gate is defined by a conductive layer covered with a first insulated material thereon and comprises a sidewall made of a second insulated material;

a floating gate aligned to said select gate;

a third insulated material disposed over said tunnel oxide layer, said select gate and said floating gate; and

a control gate formed on said third insulated material.

12. The structure according to Claim 11, wherein each of said first insulated material, said second insulated material and said third insulated

material is one selected from a group consisting of silicon oxide, silicon nitride and silicon oxide/nitride composite.

13. The structure according to claim 11, wherein said conductive layer is one selected from a group consisting of polysilicon, amorphous silicon, recrystallized silicon and polycide.

14. The structure according to claim 11, wherein each of said floating gate and said control gate is one selected from a group consisting of polysilicon, amorphous silicon and recrystallized silicon.